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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,580	12/31/2001	Howard S. David	42390.P13870	2198

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EXAMINER	
LI, ZHUO H	
ART UNIT	**PAPER NUMBER**
2186	4

DATE MAILED: 09/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/039,580	Applicant(s) DAVID, HOWARD S.	
	Examiner Zhuo H Li	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Page 6 lines 4-5, "the DRAM is placed on a motherboard rather that on a memory module" should be -- the DRAM is placed on a motherboard rather than on a memory module--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 23-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Ayukawa et al. (US PAT. 6,381,671 hereinafter Ayukawa).

Regarding claim 23, Ayukawa discloses a method receiving a read and preload command at a memory module, i.e., DRAM macro (5Ma-5Md, figure 1) from the access optimizer, reading a current line of data from at least one memory device, i.e., memory banks (1-4, figure 2), reading a next line of data from at least one memory device, pre-fetching the next line of data into a data cache, i.e., amplifier cache (55, figure 2) on the memory module (col. 12 lines 19-24, col. 13 line 47 through col. 14 line 35).

Regarding claim 24, Ayukawa discloses the read and preload command including memory module destination information, way information, address strobe state information, and cache hit information (col. 3 lines 21-33 and col. 11 line 50 through col. 12 line 43).

Regarding claim 25, Ayukawa discloses the read and preload command further including column address information and memory device bank information (col. 3 lines 21-33 and col. col. 12 lines 5-18).

Regarding claims 26-27, Ayukawa discloses the method wherein receiving the read and preload command includes receiving the read and preload command information over four transfer periods, i.e., 6 to 8 clock cycles, and includes receiving the cache hit information any way information during the fourth transfer period (figure 6 and 7 and col. 13 line 47 through col. 15 line 4).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury) in view of Ayukawa et al (US PAT. 6,381,671 hereinafter Ayukawa).

Regarding claim 1, Saulsbury discloses an apparatus (104, figure 2) comprising an array of tag address storage locations, i.e., data cache bank tag/flag storage (col. 7 lines 42-61), and a command sequencer and serializer unit, i.e., data cache bank logic (150, figure 2), coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache, i.e., data cache bank line storage (144, figure 2) associated with a memory module, i.e., memory bank N (118, figure 2) and (col. 7 line 21 through col. 8 line 1). Saulsbury differs from the claimed invention in not specifically teaches the command sequencer and serializer unit to cause a current line of data to be read out of a memory module memory device and to load a next line of data from the memory module memory device to the data cache. However, Ayukawa teaches in a semiconductor integrated circuit, having a plurality of memory device, i.e., DRAM macro (5Ma, 5Mb, 5Mc and 5Md), each of memory device comprising a plurality of memory banks (bank 1-Bank 4, figure 2), a main amplifier array, i.e., data cache (55, figure 2) and (col. 8 lines 24-34), in addition, in the semiconductor integrated circuit further comprising a command sequencer and serializer unit, i.e., access optimizer (4, figure 1), which generates

commands to each of memory banks performing memory accessing operation via bus (9ACB) (col. 8 lines 56-58), furthermore, in the access optimizer unit includes an address self-prefetching unit which generates pre-fetching command to the plurality of memory banks based on the previous read command, and which cause the next address will store in the data cache, i.e., sense amplifier array (col. 12 lines 19-24, col. 13 line 47 through col. 14 line 35). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the command sequencer and serializer unit of Saulsbury in having function to cause a current line of data to be read out of a memory module memory device and to load a next line of data from the memory module memory device to the data cache, as per teaching by the multiple memory modules system, because it enhances the hit ratio of the sense amplifier cache by next address self-prefetching, and enhances the speed of first access to a multi-bank memory.

Regarding claim 2, Saulsbury disclose the command sequencer and serializer unit to control the data cache associated with the memory module by delivering commands over a plurality of command and address lines, i.e., cache lines (4096), W/R control line, cache buffer control line and address line (A20-A9) as show in figure 2 and (col. 7 lines 21-61 and col. 9 line 54 through col. 10 line 21).

Regarding claim 3, Ayukawa discloses the command sequencer and serializer to deliver a read and preload command to the data cache associated with the memory module, the read and preload command to cause the current line of data to be read out of the memory module memory device and to load the next line of data from the memory module memory device to the data cache, i.e., in the access optimizer unit includes an address self-prefetching unit which generates pre-fetching command to the plurality of memory banks based on the previous read command,

and which cause the next address will store in the data cache, i.e., sense amplifier array (col. 12 lines 19-24, col. 13 line 47 through col. 14 line 35).

Regarding claim 4, Ayukawa discloses the read and preload command including memory module destination information, way information, address strobe state information, and cache hit information (col. 3 lines 21-33 and col. 11 line 50 through col. 12 line 43).

Regarding claim 5, Ayukawa discloses the read and preload command further including column address information and memory device bank information (col. 3 lines 21-33 and col. 11 line 50 through col. 12 line 43).

Regarding claims 6-7, Ayukawa discloses the read and preload command information delivered over four transfer periods, i.e., 6 to 8 clock cycles, and the cache hit information and way information transferred during the fourth transfer period (figure 6 and 7 and col. 13 line 47 through col. 15 line 4).

6. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury) in view of Westberg (US PAT. 5,361,391).

Regarding claim 8, Saulsbury discloses an apparatus (104, figure 2) comprising at least one memory device, i.e., memory bank N (118, figure 1) and a data cache, i.e., primary data cache bank line storage (144, figure 2) coupled to the memory device via the cache line bus (4096), the data cache controlled by a plurality of commands delivered by a memory controller component, i.e., data cache control logic (150, figure 2) via a memory bus, i.e., cache lines (4096) and control command lines as show in figure 2. Saulsbury differs from the claimed invention in not specifically teaches the memory controller component including an array of tag

address storage locations, the plurality of commands including a read and preload command. However, Westberg teaches in a computer system (10, figure 1) comprising a controller (14, figure) which including cache tag arrays (30a and 30b, figure 2) each corresponding to the address locations in memory (16, figure 2) and (col. 4 lines 34-46), and the memory controller further comprising a control logic (28, figure 2) which generates different commands which received from the CPU to perform memory operations, and which including read and pre-fetch commands (col. 4 line 6 through col. 5 line 66). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory controller of Saulsbury in having an array of tag address storage locations, the plurality of commands including a read and preload command, as per teaching by the controller of Westberg, because it reduces CPU idle time and improves the computer system performance.

Regarding claim 9, Saulsbury discloses the apparatus further comprising a command decoder and deserializer, i.e., row decoder (124, figure 2) to receive command and address information from the memory controller component via the address line (A20-A9, figure 2) and (col. 4 lines 2-4), the command decoder and deserializer unit providing control for the data cache (col. 9 line 54 through col. 10 line 21).

7. Claims 10-14 and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury) and Westberg (US PAT. 5,361,391) and further in view of Ayukawa et al (US PAT. 6,381,671 hereinafter Ayukawa).

Regarding claim 10, the combination of Saulsbury and Westberg differs from the claimed invention in not specifically teaches the read and preload command to cause a current line of data

to be read out of the memory device and to load a next line of data from the memory device to the data cache. However, Ayukawa teaches in a semiconductor integrated circuit, having a plurality of memory device, i.e., DRAM macro (5Ma, 5Mb, 5Mc and 5Md), each of memory device comprising a plurality of memory banks (bank 1-Bank 4, figure 2), a main amplifier array, i.e., data cache (55, figure 2) and (col. 8 lines 24-34), in addition, in the semiconductor integrated circuit further comprising a command sequencer and serializer unit, i.e., access optimizer (4, figure 1), which generates commands to each of memory banks performing memory accessing operation via bus (9ACB) (col. 8 lines 56-58), furthermore, in the access optimizer unit includes an address self-prefetching unit which generates pre-fetching command to the plurality of memory banks based on the previous read command, and which cause the next address will store in the data cache, i.e., sense amplifier array (col. 12 lines 19-24, col. 13 line 47 through col. 14 line 35). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Saulsbury and Westberg in having the read and preload command to cause a current line of data to be read out of the memory device and to load a next line of data from the memory device to the data cache, as per teaching of Ayukawa, because it enhances the hit ratio of the sense amplifier cache by next address self-prefetching, and enhances the speed of first access to a multi-bank memory.

Regarding claim 11, Ayukawa discloses the read and preload command including memory module destination information, way information, address strobe state information, and cache hit information (col. 3 lines 21-33 and col. 11 line 50 through col. 12 line 43).

Regarding claim 12, Ayukawa discloses the read and preload command further including column address information and memory device bank information (col. 3 lines 21-33 and col. 11 line 50 through col. 12 line 43).

Regarding claims 13-14, Ayukawa discloses the read and preload command information delivered over four transfer periods, i.e., 6 to 8 clock cycles, and the cache hit information and way information transferred during the fourth transfer period (figure 6 and 7 and col. 13 line 47 through col. 15 line 4).

Regarding claim 17, the limitations of the claim are rejected as the same reasons set forth in claim 10.

Regarding claim 18, the limitations of the claim are rejected as the same reasons set forth in claim 11.

Regarding claim 19, the limitations of the claim are rejected as the same reasons set forth in claim 12.

Regarding claims 20-21, the limitations of the claims are rejected as the same reasons set forth in claims 13-14

8. Claims 15-16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Westberg (US PAT. 5,361,391) in view of Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury).

Regarding claim 15, Westberg discloses a system (10, figure 1) comprising a processor (12, figure 1), a memory controller (14, figure 1) coupled to the processor via the address bus (22) and data bus (24), the memory controller including an array of tag address locations (30a

and 30b, figure 2 and col. 4 lines 34-46), and a command sequencer and serializer unit, i.e., control logic (28, figure 2) coupled to the array of tag address storage locations (col. 4 lines 34-59), and memory module (16, figure 2) coupled to the memory controller via the address bus (22), data bus (24) and control signal bus as show in figure 2, in addition, the memory controller is able to provide a plurality of commands which including a read and preload command, i.e., the memory controller further comprising a control logic (28, figure 2) which generates different commands which received from the CPU to perform memory operations, and which including read and pre-fetch commands (col. 4 line 6 through col. 5 line 66). Westberg differs from the claimed invention in not specifically teaches the memory module including at least one memory device and a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller. However, Saulsbury discloses the computer system (100, figure 1) comprising a memory device wherein the memory device including a plurality of memory modules, i.e., memory block (104), and the memory module further including a memory device, i.e., memory bank N (118) and a data cache (144) wherein the data cache coupled to the memory device via the cache line bus (4096, figure 2), and the data cache controlled by commands, i.e., cache line buses and buffer control buses (figure 2), delivered by the memory controller, i.e., data cache bank logic (150) and (col. 7 lines 21-41 and col. 11 line 15 through col. 12 line 6). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the computer system of Westberg in having the memory module including at least one memory device and a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory

controller, as per teaching by the system of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claims 16, Saulsbury discloses the apparatus further comprising a command decoder and deserializer, i.e., row decoder (124, figure 2) to receive command and address information from the memory controller component via the address line (A20-A9, figure 2) and (col. 4 lines 2-4), the command decoder and deserializer unit providing control for the data cache (col. 9 line 54 through col. 10 line 21).

Regarding claim 22, Saulsbury discloses a point-to-point interconnect to couple the memory controller to the memory module (figure 2, and col. 3 line 55 through col. 4 line 10).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pawlowski (US PAT. 5,787,475) discloses controlled prefetching of data requested by a peripheral (abstract).

Zangenehpour (US PAT. 5,146,578) discloses method of varying the amount of data prefetched to a cache memory in dependence on the history of data requests (abstract).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tue-Fri 9:00 a.m. to 6:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Zhuo H. Li

Art Unit 2186

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